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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,583	03/24/2005	Charles Eugene Stroud	46872/308797	9939

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EXAMINER	
PRETLOW, DEMETRIUS R	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/516,583	STROUD ET AL.	
	Examiner	Art Unit	
	Demetrius R. Pretlow	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,13,17,18,21,30 and 31* is/are rejected.

7)☒ Claim(s) *2,8-12,14-16,19,20,22-29 and 32-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 rejected under 35 U.S.C. 102(e) as being anticipated by Abramovici et al. (US 6,874,108). Abraomovici et al. teach applying a test pattern approximately simultaneously to a first path under test in the field-programmable gate array and a second path under test in the field-programmable gate array, wherein the first path under test and the second path under test have substantially the same propagation delays in a fault free circuit; Note column 2, lines 36-44 and Figure 4. Abramovici et al. teach receiving a first output signal indicating that the test pattern has propagated through at least one of the first path under test and the second path under test; Note column 2, lines 36-44 and Figure 4 and column 5, lines 23-31. Abramovici et al. teach receiving a second output signal that indicates the test pattern has propagated through each of the first path under test and the second path under test; Note column 2, lines 36-44 and Figure 4 and column 5, lines 23-31. Abramovici et al. teach determining the interval between receiving the first output signal and the second output signal; Note column 5, lines 31-36. Abramovici et al. teach identifying a fault in at least one of the

first path under test and the second path under test when the interval exceeds a threshold (matching). Note column 5, lines 34-37. Abramovici et al.teach causing an indication of the fault to be output. Note column 5, lines 37-38.

In reference to claim 3, Abramovici et al. does not explicitly teach wherein the test pattern comprises contain a high to low transition however this would be inherent to the test pattern of Abramovici et al. Note column 5, lines 25-27.

In reference to claim 4, Abramovici et al. does not explicitly teach wherein the test pattern comprises contain a low to high transition however this would be inherent to the test pattern of Abramovici et al. Note column 5, lines 25-27.

In reference to claim 5, Abramovici et al. teach generating the test pattern. Note column 5, line 18 and 19.

In reference to claim 6, Abramovici et al. teach configuring the firslt path under test and the second path under test. Note column 3, lines 50-53.

In reference to claim 7, Abramovici et al. teach developing a configuration for the first path under test and the second path under test. Note column 3, lines 50-53.

In reference to claim 13, Abramovici et al. teach an input. Note column 5, lines 24-25. Abramovici et al. teach a first path under test in the field-programmable gate array, the first path under test in communication with the input; Note Fig. 4. Abramovici et al. teach a second path under test in the field-programmable gate array, the second path in communication with the input, wherein the second path has an expected propagation delay substantially the same as the first path under test; Note Fig. 4 and column 5, lines 31-32. Abramovici et al. teach an output response analyzer in

communication with the first path and the second path and operable to determine an interval between the time a data signal propagates through the first path under test and the second path under test. Note column 5, lines 31-37.

In reference to claim 17, Abramovici et al. teach wherein the programmable logic blocks in the first path under test and the second path under test comprise identity functions. Note Abramovici et al. column 6, lines 59-64.

In reference to claim 21, Abramovici et al. teach neither of the first path under test and the second path under test comprises a flip flop. Note Figure 4.

In reference to claim 30, Abramovici et al. teach wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same vertical self-testing area (V- STAR). Note column 2, lines 23-24.

In reference to claim 31, Abramovici et al. teach wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same horizontall self-testing area (H- STAR). Note column 2, lines 23-24.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Abramovici et al. in view of Stroud et al. (US 6003150).

Abramovici et al. does not teach wherein each of the first path under test and the second path under test comprises at least one lookup table (LUT) and where each LUT is configured to produce a transition when the input of the LUT changes to a specified target address.

Stroud et al. teach wherein each of the first path under test and the second path under test comprises at least one lookup table (LUT) and where each LUT is configured to produce a transition when the input of the LUT changes to a specified target address. Note column 5, lines 52-58.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Abramovici et al. to include the teaching of Stroud et al. because it would allow the determination of undetectable faults. Note column 7, lines 51-53.

Allowable Subject Matter

Claims 2,8-12,14-16,19,20,22-29,32-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claim 2 the prior art of record does not teach the inclusion of the limitations of activating an oscillating signal after receiving the first output signal; deactivating the oscillating signal after receiving the second output signal; and counting the number of oscillation cycles occurring while the oscillating signal is active.. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 8 the prior art of record does not teach the inclusion of the limitations of the first path under test comprises a fast path; and the second path comprises a slow path.. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 9-12 the prior art of record does not teach the inclusion of the limitations of wherein at least one of the first path under test and the second path under test comprises at least one programmable logic block (PLB) configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout). It is these limitations found in each of the claims, as they are

claimed in the combination, that has not been found, taught or suggested by the prior art of record.

In reference to claims 14-16 the prior art of record does not teach the inclusion of the limitations of an oscillator; and a counter in communication with the oscillator. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 19 the prior art of record does not teach the inclusion of the limitations of wherein the LUT contents of the target address comprises a 1 and the LUT contents of all other addresses comprise a 0. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 20 the prior art of record does not teach the inclusion of the limitations of wherein the LUT contents of the target address comprises a 0 and the LUT contents of all other addresses comprise a 1. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 22 the prior art of record does not teach the inclusion of the limitations of wherein each LUT comprises k inputs and each of the first path under test and second path under test comprises consecutive groups of 2k pairs of LUT's, wherein each of the groups comprises the same configuration and each pair comprises a different target address.. It is these limitations found in each of the claims, as they are

claimed in the combination, that has not been found, taught or suggested by the prior art of record.

In reference to claim 23-29 the prior art of record does not teach the inclusion of the limitations of a first programmable logic block configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout). It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 32-33 the prior art of record does not teach the inclusion of the limitations of wherein each path under test comprises a horizontal segments contained in a H-STAR and a vertical segment contained in a V-STAR, and further comprising a configurable interconnect point configured at the intersection of the V-STAR and the H-STAR connecting the said horizontal and vertical segments. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 34 the prior art of record does not teach the inclusion of the limitations of the FPGA under test comprises a plurality of parallel vertical self-testing areas (V-STAR's), and each V-STAR comprises the delay-fault testing system of claim 13.. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claim 35 the prior art of record does not teach the inclusion of the limitations of the FPGA under test comprises a plurality of parallel vertical self-testing

areas (H-STAR's), and each H-STAR comprises the delay-fault testing system of claim 13.. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Demetrius R. Pretlow Demetrius Pretlow 11/22/06

Patent Examiner

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